UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,376	04/25/2001	Yoshikazu Satoh	PHJ 99,016	7757

24737 7590 09/07/2006

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,376	SATOH, YOSHIKAZU	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,7,9-16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7,9-16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/19/06 has been entered.

2. In response to the Office action mailed on February 28, 2005, claims 2, 5, 8, and 17 have been canceled. As a result, claims 1, 3-4, 7, 9-16, and 18 are now pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1, 3, and 15-16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Higashida et al. (6,826,181).

As per claim 1, Higashida et al. discloses a data writing/reading method of sequentially writing a plurality of data into a memory in a write direction [*the generating*

means executes the interleave process by writing the data; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39]; wherein when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction*; Fig.20, col.23, lines 38-46].

As per claim 3, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 15, Higashida et al. discloses a memory for sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus*

having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix; col.3, lines 35-39].

As per claim 16, Higashida et al. discloses a memory drive apparatus [*transmission and storage apparatus*; col.3, lines 45-48]; sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

As per claim 18, Higashida et al. discloses the apparatus provides with addressing means for addressing the memory [*the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67]; plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 6-7, and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashida et al. (6,826,181) in view of Biro et al. (5,995,080).

As per claim 4, the rationale in the rejection of claim 1 above is herein incorporated. Higashida et al. further discloses a data writing/reading method of sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks*

(plurality of data); col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

However Higashida et al. does not specifically teach a method of de-interleaving. Biro et al. discloses a method of de-interleaving [*a method for providing de-interleaving of data using a storage device*; col.2, lines 63-65] to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12).

Since the technology for implementing a storage system with a method of de-interleaving was well known as evidenced by Biro et al., and since a method of de-interleaving in a storage system provides output data that is stored in an interleaved

format to other logic in a block format while using a minimal amount of additional hardware, an artisan would have been motivated to implement this feature in the system of Higashida et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made by applicant, to modify the system of Higashida et al. to include a method of de-interleaving because it was well known to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12) as taught by Biro et al..

As per claim 6, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 7, the rationale in the rejection of claim 1 above is herein incorporated. Higashida et al. further discloses a data processing method (Fig.4, *data processing circuit 104*; col.6, lines 42-43; *the transmission can be achieved by executing the process twice;* col.22, lines 33-34]; a first step of interleaving a plurality of data [*data into a plurality of blocks; a first processing means for executing a first interleave process*; col.3, lines 43-47]; sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in*

a first direction (write direction of Fig.21 (C); col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

However, Higashida et al. does not specifically teach a second step of de-interleaving. Biro et al. discloses a second step of de-interleaving [to *provide de-interleaving, the first order of bytes includes a plurality of interleaved bytes of different types of data, and the second output order of bytes comprises a plurality of bytes of the same type of data;* col.3, lines 1-4] to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12).

Since the technology for implementing a storage system with a second step of de-interleaving was well known as evidenced by Biro et al., and since a second step of

de-interleaving in a storage system provides output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware, an artisan would have been motivated to implement this feature in the system of Higashida et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made by applicant, to modify the system of Higashida et al. to include a second step of de-interleaving because it was well known to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12) as taught by Biro et al..

As per claim 9, Higashida discloses the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix form, and contains interleaving the plural data configuring the super frame [*execute the interleave process by writing data into a storage having a matrix form*; col.3, lines 34-37; *a first interleave processing means for executing a first interleave process by writing data into a first storage having a first matrix form; second interleave processing means for executing a second interleave process by writing data into a second storage having a second matrix form; each storage (frame) stores matrix/matrices which store(s) plural data*; col3, lines 46-61].

As per claim 10, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of

each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 11, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction*; Fig.20, col.23, lines 38-46].

Regarding claim 11, although Higashida et al. and Biro et al. do not specifically teach each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data, such limitations are merely a matter of design choice and would have been obvious in the system of Higashida et al.. Higashida et al. teaches a two-dimensional matrix, and the frames become the multiple of 48 bytes to execute the interleave process and express data write and read control. The limitations in claim 11 do not define a patentably distinct invention over that in Higashida et al. since both the invention as a whole and Higashida et al. are directed to configuring and interleaving

the super frame. The size of the data in the matrix is inconsequential for the invention as a whole and presents no new or unexpected results, as long as the data is in matrix form. Therefore, to have each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data would have been a matter of obvious design choice to one of ordinary skill in the art.

As per claims 12-14, the rationale in the rejection of claim 10 is herein incorporated.

Regarding claims 12-14, although Higashida et al. and Biro et al. do not specifically teach a super frame having eight frames, each of the frames formed by arranging (203x48) data in matrix form, interleaving (203x48x8) data, and each block having 4 or 26 addresses, such limitations are merely a matter of design choice and would have been obvious in the system of Higashida et al.. Higashida et al. teaches a two-dimensional matrix, and the frames become the multiple of 48 bytes, to execute the interleave process and express data write and read control, and control circuit 1003 generates an address to sequentially read the data in the row direction of the matrix. The limitations in claims 12-14 do not define a patentably distinct invention over that in Higashida et al. since both the invention as a whole and Higashida et al. are directed to configuring, interleaving the super frame, and sequentially reading the data. The size of the data in the matrix is inconsequential for the invention as a whole and presents no new or unexpected results, as long as the data is in matrix form. Therefore, to have

each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data would have been a matter of obvious design choice to one of ordinary skill in the art.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Higashida et al.	6,826,181
Biro et al.	5,995,080
Norbert et al.	3,271,749

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 4, 2006

Mardochee Chery
Examiner
AU: 2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
9/6/06